REMARKS

Claims 1, 2, 4-6, 13, 14 and 16-20 are pending in the present application. Claims 1, 2, 13, 14 and 20 have been amended. Claims 3 and 15 have been canceled.

Claim Objections

Claims 1-6 and 13-20 have been objected to in view of the informalities as listed on page 2 of the current Office Action dated March 10, 2006. The Examiner has asserted that the present application does not specifically describe impurity **diffused** source/drain regions as featured in claims 1 and 13. This objection is respectfully traversed for the following reasons.

As described on page 11, lines 16-19 of the application, polysilicon layer 43 is shown in Fig. 9B as formed on the source/drain portions, and resist 45 is then formed followed by source/drain implantation. Thereafter, an activating RTA (rapid thermal anneal) is affected, and then resist 45 is removed, to provide the structure as shown in Fig. 10A.

Applicant respectfully submits that the activating RTA diffuses impurities into SOI layer 33 in view of the heat treatment. Claim 1 has thus been amended to feature that the thin silicon layer includes a channel region and "an impurity activated source/drain region". Claim 13 has been amended in a somewhat similar manner. The Examiner is respectfully requested to withdraw the objection to the claims for at least these reasons.

Claim Rejections-35 U.S.C. 102

Claims 1-5, 13-17, 19 and 20 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Wakahara et al. reference (Japanese Patent Publication No. 2000-183355). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The full depletion SOI-MOS transistor of claim 1 includes in combination a substrate; a buried oxide layer; a thin silicon layer; an isolation layer "on the buried oxide layer, the isolation layer adjacent the thin silicon layer"; a gate insulation layer; a gate electrode; and a deposited polysilicon layer "on the impurity activated source/drain region of the thin silicon layer and extending on an uppermost surface of the isolation layer, wherein the impurity activated source/drain region and the deposited polysilicon layer together constitute a source/drain of the full depletion SOI-MOS transistor". Applicant respectfully submits that the Wakahara et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has interpreted layer 13b and layer 4 in Fig. 11 of the Wakahara et al. reference for example, respectively as the deposited polysilicon layer and the isolation layer of claim 1. However, layer 13B in Fig. 11 of the Wakahara et al. reference merely abuts against a side surface of layer 4, and does not extend on an uppermost surface of the isolation layer. The Wakahara et al. reference as relied upon by the Examiner does not disclose these features. Since the deposited polysilicon layer of claim 1 extends on an uppermost surface of the isolation layer, a subsequently

formed upper metal layer can surely and easily contact the deposited polysilicon layer in a reliable manner. Applicant therefore respectfully submits that the full depletion SOI-MOS transistor of claim 1 distinguishes over the Wakahara et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1, 2, 4 and 5 is improper for at least these reasons.

The full depletion SOI-MOS transistor of claim 13 includes in combination a substrate, a BOX layer; an SOI layer; an isolation layer "on the BOX layer, the isolation layer adjacent the SOI layer"; a gate insulation layer; a gate electrode; and a deposited high mobility conductive layer "on the impurity activated source/drain region of the thin silicon layer and extending on an uppermost surface of the isolation layer, wherein the deposited high mobility conductive layer contains polysilicon and wherein the impurity activated source/drain region and the deposited high mobility conductive layer together constitute a source/drain of the full depletion SOI-MOS transistor".

Applicant respectfully submits that the Wakahara et al. reference as relied upon by the Examiner does not disclose the above note features of claim 13. As emphasized previously, layer 13b in Fig. 11 of the Wakahara et al. reference merely abuts against a side surface of layer 4, and does not extend on an uppermost surface of layer 4. Accordingly, Applicant respectfully submits that the full depletion SOI-MOS transistor of claim 13 distinguishes over the Wakahara et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 13-17, 19 and 20, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 6 and 18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Wakahara et al. reference in view of the Cheng et al. reference (U.S. Patent Application Publication No. 2002/0171107). Applicant respectfully submits that the Cheng et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the primarily relied upon Wakahara et al. reference. Accordingly, Applicant respectfully submits that claims 6 and 18 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together for at least these reasons.

Conclusion

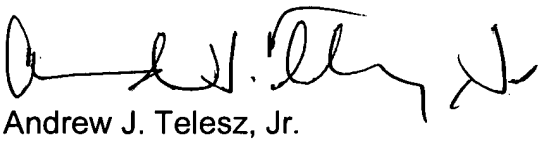
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740